

TABLE 1-continued

Dielectric Material	Approximate Relative Permittivity (K)
barium titanate (BaTiO_3)	~20—200
strontium titanate SrTiO_3	~20—200
PbZrO_3	~20—200
PST ($\text{PbSc}_x\text{Ta}_{1-x}\text{O}_3$)	3000
PZN ($\text{PbZn}_x\text{Nb}_{1-x}\text{O}_3$)	~500—5000
PZT ($\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$)	~150—1000
PMN ($\text{PbMg}_x\text{Nb}_{1-x}\text{O}_3$)	~500—5000

It is noted that the K-values for both standard-K and high-K materials may vary to some degree depending on the exact nature of the dielectric material. Thus, for example, differences in purity, crystallinity and stoichiometry, may give rise to variations in the exact K-value determined for any particular dielectric material.

As used herein, when a material is referred to by a specific chemical name or formula, the material may include non-stoichiometric variations of the stoichiometrically exact formula identified by the chemical name. For example, tantalum oxide, when stoichiometrically exact, has the chemical formula Ta_2O_5 , but may include variants of stoichiometric Ta_2O_5 , which may be referred to as Ta_xO_y , in which either of x or y vary by a small amount. For example, in one embodiment, x may vary from about 1.5 to 2.5, and y may vary from about 4.5 to about 5.5. In another embodiment, x may vary from about 1.75 to 2.25, and y may vary from about 4 to about 6. Such variations from the exact stoichiometric formula fall within the definition of tantalum oxide. Similar variations from exact stoichiometry for all chemical names or formulas used herein are intended to fall within the scope of the present invention. For example, again using tantalum oxide, when the formula Ta_2O_5 is used, Ta_xO_y is included within the meaning. Thus, in the present disclosure, exact stoichiometry is intended only when such is explicitly so stated. As will be understood by those of skill in the art, such variations may occur naturally, or may be sought and controlled by selection and control of the conditions under which materials are formed.

With continued reference to FIGS. 2 and 3D, the method 60 continues in step 102 where a layer of gate electrode material 104 is formed over the layer of high-K material 100. The gate electrode material 104 can be deposited by chemical vapor deposition (CVD). In one embodiment, the gate electrode material 104 is deposited to overfill the space between the TEOS layer 80. In the illustrated embodiment, the gate 28 has a length adjacent the body 14 such that the deposition of about 250 Å of gate electrode material 104 will fill the recess 90 and establish the T-shaped gate electrode 32 configuration. The use of CVD to deposit the layer of gate electrode material 82 is advantageous to minimize the introduction of additional interface charge.

As indicated above, the layer of gate electrode material 104 can be composed of a metal (e.g., tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum, titanium, molybdenum, etc) or a metal containing compound (e.g., titanium nitride, tantalum nitride, ruthenium oxide, etc.). If desired, a semiconductor (e.g., polycrystalline silicon, polycrystalline silicon-germanium, etc.) could also be used. The gate electrode material layer 104 can be selected for N-channel devices (e.g., tungsten, tantalum, aluminum, titanium nitride, tantalum nitride) or for P-channel devices (e.g., tungsten, nickel, ruthenium, rhodium, palladium, platinum, titanium nitride, tantalum nitride or ruthenium oxide).

Thereafter, in step 106 and with additional reference to FIG. 3E, the layer of gate electrode material 104 and the layer of high-K material 100 can be polished (using, for example, CMP) to remove portions of the layer of gate electrode material 104 and the layer of high-K material 100 that are disposed over the layer 44. As illustrated, the layer 80 and the configuring layer 44 act to define the shape of an upper portion of the gate 28 to result in a T-shaped gate. Next, in step 108, the TEOS oxide layer 44 can be removed, such as by wet chemical etching in hydrofluoric (HF) acid.

Next, in step 110 and with reference back to FIG. 1, the source 22 and the drain 24 can be opened. Opening the source 22 and the drain 24 can include removing portions of the configuring layer 44 and the liner 46 extending laterally beyond the arms 40 of the gate 28 and exposed by removal of the TEOS layer 80. In the illustrated embodiment where the configuring layer 44 is made from nitride, the configuring layer 44 and/or the liner 46 can be patterned in step 110 using RIE. Alternatively, wet chemical etching can be used to open the source 22 and the drain 24.

Next, in step 112, the source contact 48 and the drain contact 50 are formed. In the illustrated embodiment, the source contact 40 and the drain contact 50 are formed from silicide. Briefly, the silicide can be formed by depositing a layer of metal (such as cobalt, nickel, molybdenum or titanium) and reacting the metal with the layer of semiconductor material 16. Without intending to be bound by theory, it is believed that a quality high-K gate dielectric can be obtained if silicidation (or salicidation) of the source 22 and the drain 24 is carried out after gate 28 formation. In addition, possible contamination issues can be minimized (such contamination issues being specific to the materials and processing techniques used).

The method 60 can continue in step 114 where any additional processing to complete the formation of the semiconductor device 10 and to interconnect devices formed on the wafer 12 can be carried out. Such additional processing can include steps to form, for example, a cap layer, contact holes or vias, conductor runs and so forth.

The method 60 shows a specific order of steps for fabricating the semiconductor device 10. However, it is understood that the order may differ from that depicted. For example, the order of two or more steps may be altered relative to the order shown. Also, two or more steps may be carried out concurrently or with partial concurrence. In addition, various steps may be omitted and other steps may be added. Furthermore, the method 60 can be modified for the formation of devices other than the illustrated MOSFET. It is understood that all such variations are within the scope of the present invention.

With reference to FIG. 4, an alternative embodiment of the semiconductor device 10 (FIG. 1) is illustrated. It is noted that in FIG. 4, components of the semiconductor device 10' have been given the same reference numerals as counterpart components of the semiconductor device 10 illustrated in FIG. 1, but with a prime symbol (') added thereto. As indicated above, the semiconductor device 10' is made by removing portions of the liner 46 that were disposed adjacent the dummy gate 66 before formation of the spacers 38'. In the illustrated embodiment, the configuring layer 44 and the spacers 38' are each formed from a nitride and are thus shown without demarcation.

With reference to FIG. 5, another alternative embodiment of the semiconductor device 10 (FIG. 1) is illustrated. It is noted that in FIG. 5, components of the semiconductor device 10" have been given the same reference numerals as

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7

Next, in step 82 and with additional reference to FIG. 3C, a portion of the configuring layer 44 is removed to provide structural surfaces 84 upon which the arms 40 of the gate 28 can be formed. In the illustrated embodiment, about 600 Å of the configuring layer 44 can be removed. If nitride is selected as the material for the configuring layer, a hot phosphoric acid etch can be used to remove the undesired portion of the configuring layer 44.

Also in step 82, a portion of the liner 46 can be removed to remove oxide that is formed over the dummy gate 66. In one embodiment, portions of the liner 46 that become exposed after patterning of the conforming layer 44 can be removed by a hydrofluoric (HF) acid dip.

Thereafter, in step 86, the dummy gate 66 is removed. In the illustrated embodiment, the dummy gate 66 includes a layer 68 of polycrystalline silicon which can be removed using a reactive ion etch (RIE) etch carried out for about ten seconds to about twenty seconds. The dummy gate 66 can also include the underlying oxide layer 70 that can also be removed with an appropriate etch technique.

Thereafter, in step 88, the layer of semiconductor material 16 is etched to form a recess 90 in which the gate 28 will be formed as described below in greater detail. In the illustrated embodiment where the layer of semiconductor material 16 is formed from silicon, the layer of semiconductor material 16 can be etched using RIE so that about 50 Å to about 100 Å of silicon remains over the isolating layer 18 (e.g., an RIE carried out for about six seconds to about twelve seconds). Alternatively, wet chemical etching such as with ammonium hydroxide (e.g., NH_4OH) can be used.

The amount of remaining semiconductor material will depend on the desired end thickness of the body region 14 following the completion of subsequent processing steps described below that may consume additional portions of the semiconductor material from the layer of semiconductor material 16. In the illustrated embodiment, the layer of semiconductor material 16 has an initial thickness of about 400 Å. Therefore, in the illustrated embodiment, about 300 Å to about 350 Å of semiconductor material can be removed from the layer of semiconductor material 16.

Next, in step 92, the layer of semiconductor material 16 is oxidized to form the oxide layer 38. The oxide layer 38 is formed from exposed portions of the layer of semiconductor material 16 and extends from a portion of the liner 46 disposed over the source 22 to a portion of the liner 46 disposed over the drain 24. One reason for oxidizing the etched surface of the layer of semiconductor material 16 is to reduce the number of defects that may be caused by etching of the layer of semiconductor material 16.

In addition, oxidizing the layer of semiconductor material 16 is carried out to further reduced the amount of semiconductor material disposed over the insulating layer 18 in the area of the body 14. In the illustrated embodiment, the oxide layer 38 can be about 25 Å to about 50 Å thick. The oxide layer 38 can be formed, for example, by exposing the wafer to heat (e.g., about 800° C. to about 850° C.) in an oxygen containing atmosphere. The resulting thickness of the body 14 will enable the semiconductor device 10 to be fully depleted.

Next, in step 94, the spacers 36 are formed. The spacers 36 can be formed by depositing a layer of desired material to a thickness of about 100 Å to about 150 Å or, alternatively, to overfill the recess 90. In either case, such a deposited layer can conform to side walls of the liner 46. Alternatively, and as illustrated in FIG. 4, portions of the liner 46 that were disposed adjacent sidewalls of the dummy

8

gate 66 can be removed in step 86 when the underlying oxide layer 70 was removed. In this alternative arrangement, the spacer material can be deposited adjacent side walls of the configuring layer 44.

In one embodiment, the material used for the spacers 36 is a nitride (e.g., silicon nitride). The deposited material can then be polished to have an upper surface generally even with the upper surface of the TEOS oxide layer 44. Next, the material can be anisotropically etched back to the oxide layer 38.

Thereafter, in step 96 and with additional reference to FIG. 3D, a portion of the oxide layer 38 formed between the spacers 36 can be removed, such as by wet chemical etching. Accordingly, the oxide layer 38 can be considered to be a sacrificial layer.

It is noted that the portion of the oxide layer 28 can alternatively be kept in place (and thinned, if desired) to serve as a buffer interface for the gate dielectric 34. In yet another alternative embodiment, the oxide layer 38 can be removed between the spacers 38 and replaced by another desired layer, including another oxide layer. The formation of another oxide layer can be used, for example, to finely tune the thickness of the body 14 and/or to form a buffer interface. In one example, the layer of semiconductor material 16 can be oxidized to consume additional semiconductor material, such as by a low temperature (about 500° C.) thermal oxidation process. In another example, oxide material can be deposited, such as by a remote plasma deposition process, an atomic layer deposition (ALD) process or the like. A deposited layer, in most circumstances, would be formed as a conformal layer such that oxide would also be formed on exposed surfaces of the TEOS layer 80, the configuring layer 66, the liner 46 and the spacers 36. Such oxide could be selectively removed or left in place.

Next, in step 98, a layer of high-K material 100 can be formed. The layer of high-K material 100 is used to form the gate dielectric 34. The layer of high-K material 100 can be deposited as a conformal layer over the layer 80, the layer 44, the spacers 36 and the exposed portion of the layer of semiconductor material 16 between the spacers 36 (or, if present, over a buffer interface formed between the spacers 36). Exemplary high-K materials are identified below in Table 1. It is noted that Table 1 is not an exhaustive list of high-K materials and other high-K materials may be available.

TABLE 1

Dielectric Material	Approximate Relative Permittivity (K)
aluminum oxide (Al_2O_3)	9-10
zirconium silicate	12
hafnium silicate	15
hafnium silicon oxynitride	16
hafnium silicon nitride	18
lanthanum oxide (La_2O_3)	20-30
hafnium oxide (HfO_2)	40
zirconium oxide (ZrO_2)	25
cerium oxide (CeO_2)	26
bismuth silicon oxide ($\text{Bi}_4\text{Si}_2\text{O}_{12}$)	35-75
titanium dioxide (TiO_2)	30
tantalum oxide (Ta_2O_5)	26
tungsten oxide (WO_3)	42
yttrium oxide (Y_2O_3)	20
lanthanum aluminum oxide (LaAlO_3)	25
barium strontium titanate ($\text{Ba}_{1-x}\text{Sr}_x\text{TiO}_3$)	~20-200
barium strontium oxide ($\text{Ba}_{1-x}\text{Sr}_x\text{O}_3$)	~20-200
PbTiO_3	~20-200

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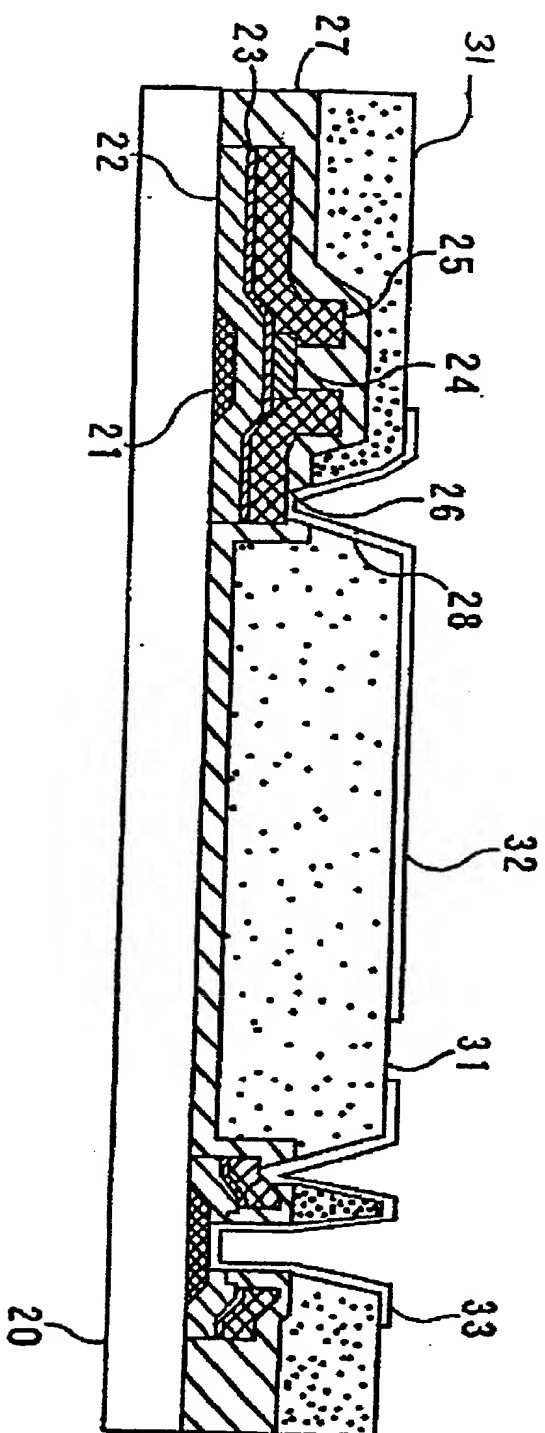


FIG. 1